

Title	Page	Manual Part	Page
Cover Sheet	1	Power Map	36
Block Diagram	2	GPIO Map	37
CPU-CLK/Control/MISC/PEG	3	Power Sequence	38
CPU-Memory	4	History	39
CPU-Power	5		
CPU-GND	6		
DDR III DIMM 1	7		
DDR III DIMM 2	8		
PPT-PCI/E/DMI/CLK/USB20&30	9		
PPT-SATA/HOST/GPIO/VGA/CCMOS	10		
PPT-SMB/LPC/AUDIO/RTC/SPI	11		
PPT-POWER	12		
PPT-GND	13		
PPT Strap	14		
PCIE1(X16)	15		
LAN1 - RTL8111E/8105E	16		
LAN2 - RTL8111E/8105E	17		
AUDIO 892	18		
SATA & Mini PCIE Connector	19		
DP Connector	20		
DVI-I Connector	21		
HDMI Connector	22		
Rear I/O & USB2.0 Connector	23		
USB3.0 Connector	24		
SIO-Fintek F71878AD	25		
FAN Controllor	26		
ATX F_Panel/EMI/TPM	27		
ACPI Controller UPI	28		
VRM12 - UT501	29		
UP6282 2-Phase+MOS CPU	30		
UP6282 1-PhaseMOS GPU	31		
UP1504T - VTT POWER	32		
UP1504T - DDR POWER	33		
XDP / Manual Parts	34		
EMI CAP	35		

MS-7733 Ver: 4.0 Mini ITX

Intel -MahoBay plamform

CPU:
INTEL-Ivy bridge LGA1155

System Chipset:

INTEL-Panther Point

OnBoard Chipset:

HD Audio Codec:RTL892
LAN-RTL8111E Co-lay 8105E
SIO:Fintek F71878AD
Flash ROM: 64 Mb SPI (CHIP)

Main Memory:

SO-DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PWM:

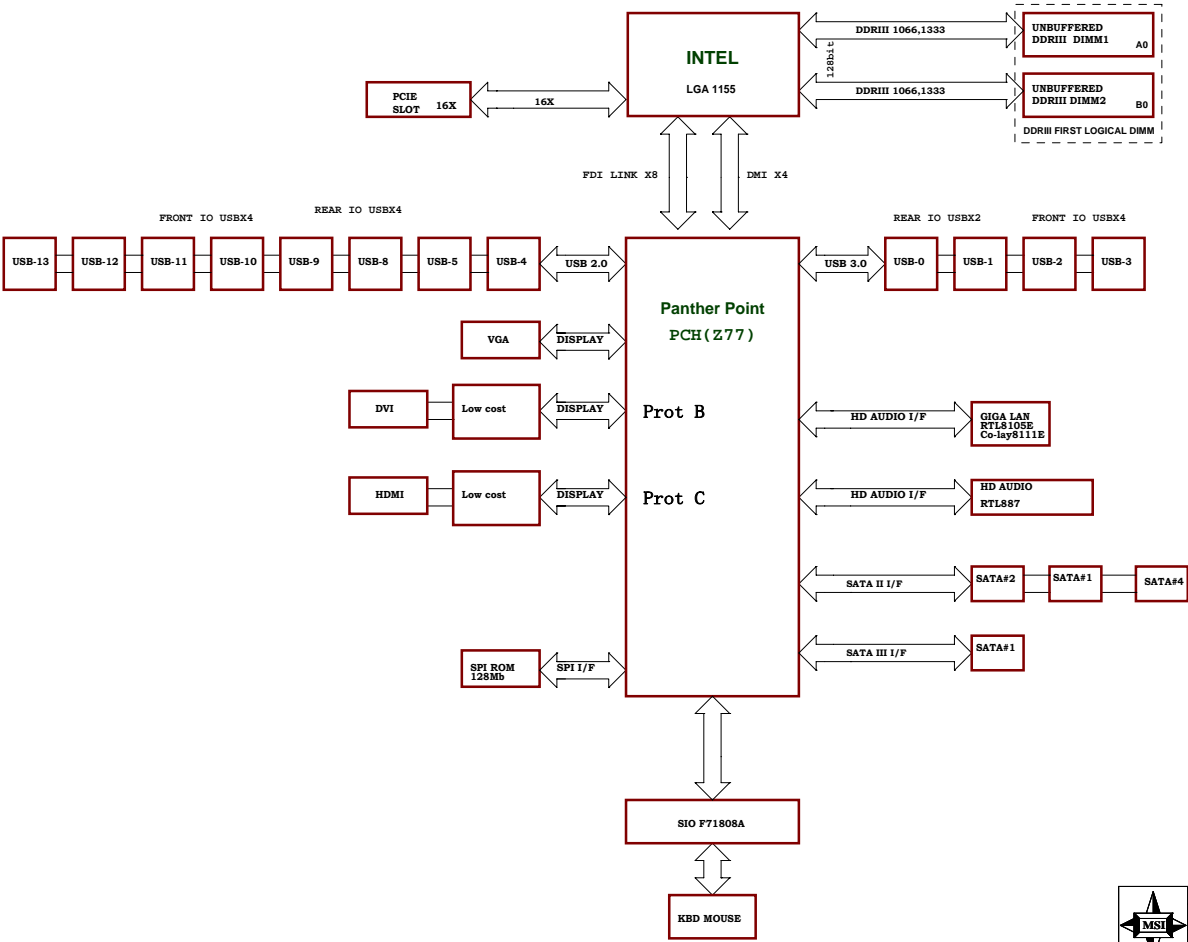
VRD12 - UT501+3Phase

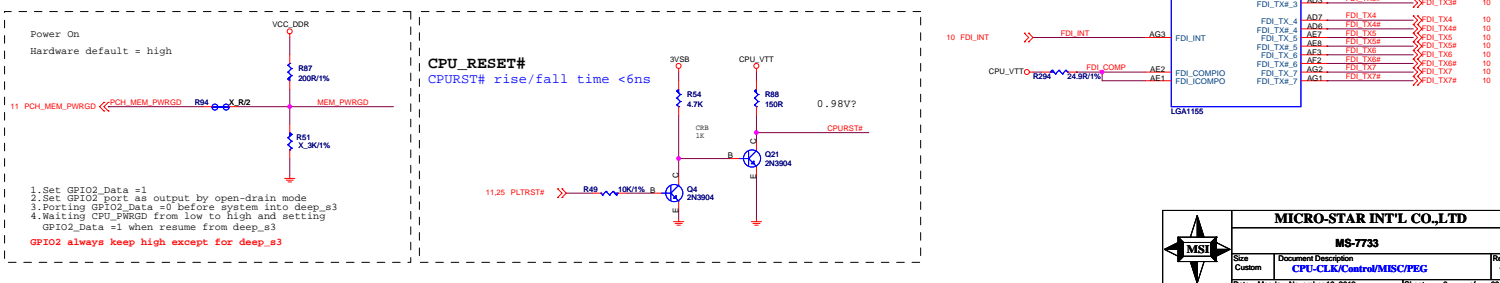
ACPI:

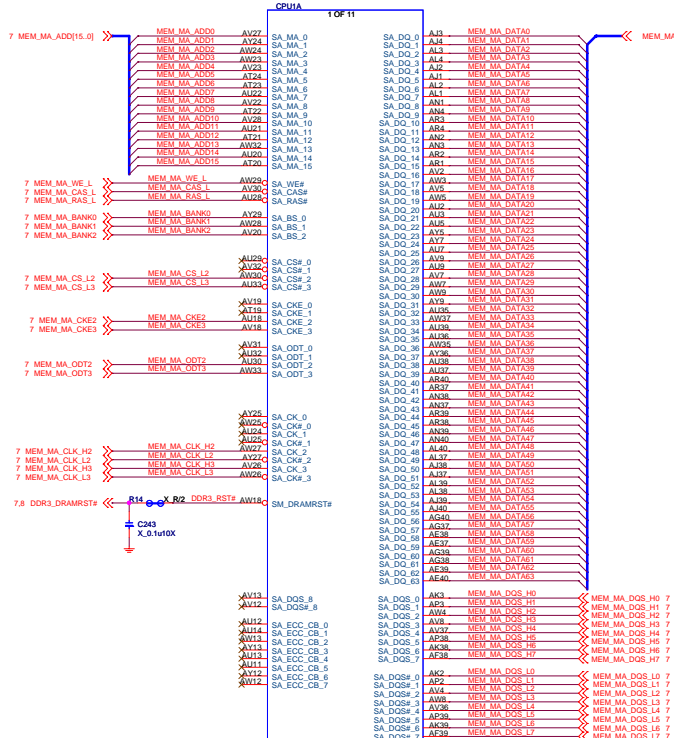
UPI

Other:

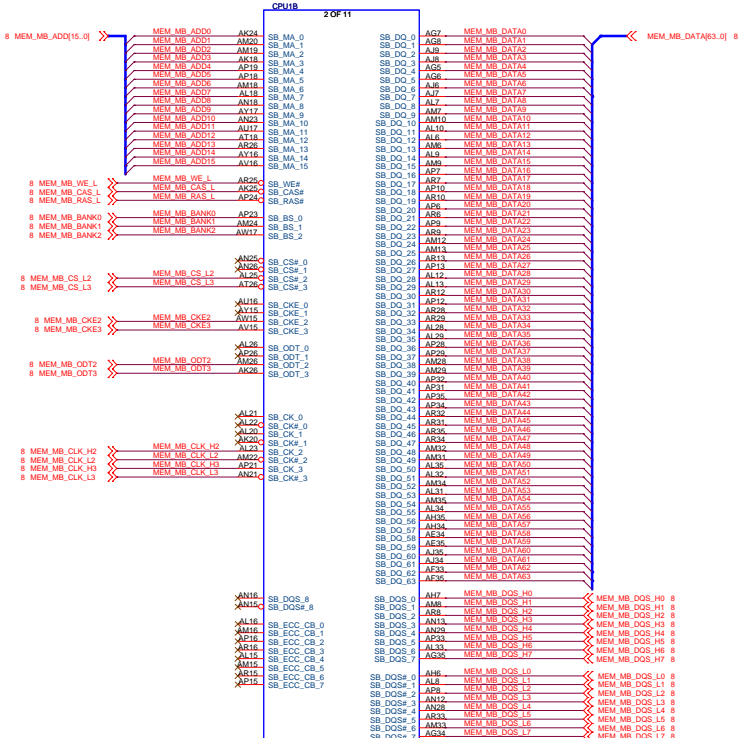
SATA(SATA2-300MB/s*2 + SATA3-600MB/s *2)
Rear USB2.0 *4+ Front USB2.0*2
REAL USB3.0 *2
FRONT USB3.0 *2







LGA1155



LGA1155

CPU#1
9 OF 11

A17	VSS_001	VSS_091	AM27
A20	VSS_002	VSS_092	AM27
A26	VSS_003	VSS_093	AM27
A30	VSS_004	VSS_094	AM27
A33	VSS_005	VSS_095	AM27
A34	VSS_006	VSS_096	AM27
A34	VSS_007	VSS_097	AM27
A35	VSS_008	VSS_098	AM27
A35	VSS_009	VSS_099	AM27
A37	VSS_010	VSS_100	AM27
A38	VSS_011	VSS_101	AM27
AM6	VSS_012	VSS_102	AM27
AM6	VSS_013	VSS_103	AM27
AC1	VSS_014	VSS_104	AM27
AC2	VSS_015	VSS_105	AM27
AD31	VSS_016	VSS_106	AM27
AD36	VSS_017	VSS_107	AM27
AD38	VSS_018	VSS_108	AM27
AD39	VSS_019	VSS_109	AM27
AD39	VSS_020	VSS_110	AM27
AD5	VSS_021	VSS_111	AM27
AD8	VSS_022	VSS_112	AM27
AE3	VSS_023	VSS_113	AM27
AE34	VSS_024	VSS_114	AM27
AE36	VSS_025	VSS_115	AM27
AF1	VSS_026	VSS_116	AM27
AF36	VSS_027	VSS_117	AM27
AF37	VSS_028	VSS_118	AM27
AF39	VSS_029	VSS_119	AM27
AF39	VSS_030	VSS_120	AM27
AF39	VSS_031	VSS_121	AM27
AF39	VSS_032	VSS_122	AM27
AF39	VSS_033	VSS_123	AM27
AG36	VSS_034	VSS_124	AM27
AG39	VSS_035	VSS_125	AM27
AH3	VSS_036	VSS_126	AM27
AH3	VSS_037	VSS_127	AM27
AH36	VSS_038	VSS_128	AM27
AH38	VSS_039	VSS_129	AM27
AH39	VSS_040	VSS_130	AM27
AH40	VSS_041	VSS_131	AM27
AH40	VSS_042	VSS_132	AM27
AH5	VSS_043	VSS_133	AM27
AH5	VSS_044	VSS_134	AM27
AH12	VSS_045	VSS_135	AM27
AH5	VSS_046	VSS_136	AM27
AH18	VSS_047	VSS_137	AM27
AC1	VSS_048	VSS_138	AM27
AH25	VSS_049	VSS_139	AM27
A26	VSS_050	VSS_140	AM27
A37	VSS_051	VSS_141	AM27
AK1	VSS_052	VSS_142	AM27
AK10	VSS_053	VSS_143	AM27
AK13	VSS_054	VSS_144	AM27
AK13	VSS_055	VSS_145	AM27
AK14	VSS_056	VSS_146	AM27
AK16	VSS_057	VSS_147	AM27
AK22	VSS_058	VSS_148	AM27
AK28	VSS_059	VSS_149	AM27
AK31	VSS_060	VSS_150	AM27
AK32	VSS_061	VSS_151	AM27
AK34	VSS_062	VSS_152	AM27
AK36	VSS_063	VSS_153	AM27
AK36	VSS_064	VSS_154	AM27
AK36	VSS_065	VSS_155	AM27
AK37	VSS_066	VSS_156	AM27
AK4	VSS_067	VSS_157	AM27
AK40	VSS_068	VSS_158	AM27
AK5	VSS_069	VSS_159	AM27
AK6	VSS_070	VSS_160	AM27
AK7	VSS_071	VSS_161	AM27
AK8	VSS_072	VSS_162	AM27
AK9	VSS_073	VSS_163	AM27
AL1	VSS_074	VSS_164	AM27
AL14	VSS_075	VSS_165	AM27
AL17	VSS_076	VSS_166	AM27
AL19	VSS_077	VSS_167	AM27
AL4	VSS_078	VSS_168	AM27
AL7	VSS_079	VSS_169	AM27
AL30	VSS_080	VSS_170	AM27
AL36	VSS_081	VSS_171	AM27
AL5	VSS_082	VSS_172	AM27
AM1	VSS_083	VSS_173	AM27
AM11	VSS_084	VSS_174	AM27
AM14	VSS_085	VSS_175	AM27
AM2	VSS_086	VSS_176	AM27
AM21	VSS_087	VSS_177	AM27
AM23	VSS_088	VSS_178	AM27
AM28	VSS_089	VSS_179	AM27
AM29	VSS_090	VSS_180	AM27

LGAT155

CPU#1
10 OF 11

AV11	VSS_181	VSS_281	H37
AV14	VSS_182	VSS_282	H37
AM30	VSS_183	VSS_283	H37
AM36	VSS_184	VSS_284	H37
AM36	VSS_185	VSS_285	H37
AV6	VSS_186	VSS_286	H37
AV6	VSS_187	VSS_287	H37
AW10	VSS_188	VSS_288	H37
AW11	VSS_189	VSS_289	H37
AW14	VSS_190	VSS_290	H37
AW16	VSS_191	VSS_291	H37
AW36	VSS_192	VSS_292	H37
AW36	VSS_193	VSS_293	H37
AV11	VSS_194	VSS_294	H37
AV14	VSS_195	VSS_295	H37
AV18	VSS_196	VSS_296	H37
AV36	VSS_197	VSS_297	H37
AV4	VSS_198	VSS_298	H37
AV5	VSS_199	VSS_299	H37
AV6	VSS_200	VSS_300	H37
B10	VSS_201	VSS_301	K23
B13	VSS_202	VSS_302	K23
B14	VSS_203	VSS_303	K33
B17	VSS_204	VSS_304	K33
B23	VSS_205	VSS_305	K37
B26	VSS_206	VSS_306	K39
B29	VSS_207	VSS_307	K5
B36	VSS_208	VSS_308	L10
B39	VSS_209	VSS_309	L17
B6	VSS_210	VSS_310	L20
B6	VSS_211	VSS_311	L20
CP11	VSS_212	VSS_312	L23
CP14	VSS_213	VSS_313	L23
C17	VSS_214	VSS_314	L29
C20	VSS_215	VSS_315	L4
C23	VSS_216	VSS_316	M1
C26	VSS_217	VSS_317	M1
C32	VSS_218	VSS_318	M2
C36	VSS_219	VSS_319	M23
C39	VSS_220	VSS_320	M7
C8	VSS_221	VSS_321	M29
D17	VSS_222	VSS_322	M39
D2	VSS_223	VSS_323	M39
D2	VSS_224	VSS_324	M39
D30	VSS_225	VSS_325	M37
D33	VSS_226	VSS_326	M39
D36	VSS_227	VSS_327	M9
D39	VSS_228	VSS_328	M9
D39	VSS_229	VSS_329	M9
D39	VSS_230	VSS_330	M9
D4	VSS_231	VSS_331	P2
D6	VSS_232	VSS_332	P46
D6	VSS_233	VSS_333	P38
E11	VSS_234	VSS_334	P38
E12	VSS_235	VSS_335	P38
E12	VSS_236	VSS_336	P39
E16	VSS_237	VSS_337	P6
E20	VSS_238	VSS_338	R33
E23	VSS_239	VSS_339	R36
E26	VSS_240	VSS_340	R37
E29	VSS_241	VSS_341	R39
E36	VSS_242	VSS_342	R8
E7	VSS_243	VSS_343	T2
F4	VSS_244	VSS_344	T6
F1	VSS_245	VSS_345	U8
F10	VSS_246	VSS_346	U8
F14	VSS_247	VSS_347	V1
F14	VSS_248	VSS_348	V2
F14	VSS_249	VSS_349	V33
F17	VSS_250	VSS_350	Y4
F2	VSS_251	VSS_351	V35
F20	VSS_252	VSS_352	V36
F23	VSS_253	VSS_353	V37
F26	VSS_254	VSS_354	V39
F29	VSS_255	VSS_355	V39
F37	VSS_256	VSS_356	V39
F39	VSS_257	VSS_357	V39
F39	VSS_258	VSS_358	Y8
F8	VSS_259	VSS_359	Y8
FL	VSS_260	VSS_360	Y8
CP1	VSS_261	VSS_361	Y8
G11	VSS_262	VSS_362	Y8
G17	VSS_263	VSS_363	Y8
G20	VSS_264	VSS_364	Y8
G23	VSS_265	VSS_365	Y8
G26	VSS_266	VSS_366	Y8
G29	VSS_267	VSS_367	Y8
G36	VSS_268	VSS_368	Y8
G7	VSS_270	VSS_370	Y8
G8	VSS_271	VSS_371	Y8
H1	VSS_272	VSS_372	Y8
H17	VSS_273	VSS_373	Y8
H2	VSS_274	VSS_374	Y8
H20	VSS_275	VSS_375	Y8
H33	VSS_276	VSS_376	Y8
H36	VSS_277	VSS_377	Y8
H39	VSS_278	VSS_378	Y8
H33	VSS_279	VSS_379	Y8
H35	VSS_280	VSS_380	Y8

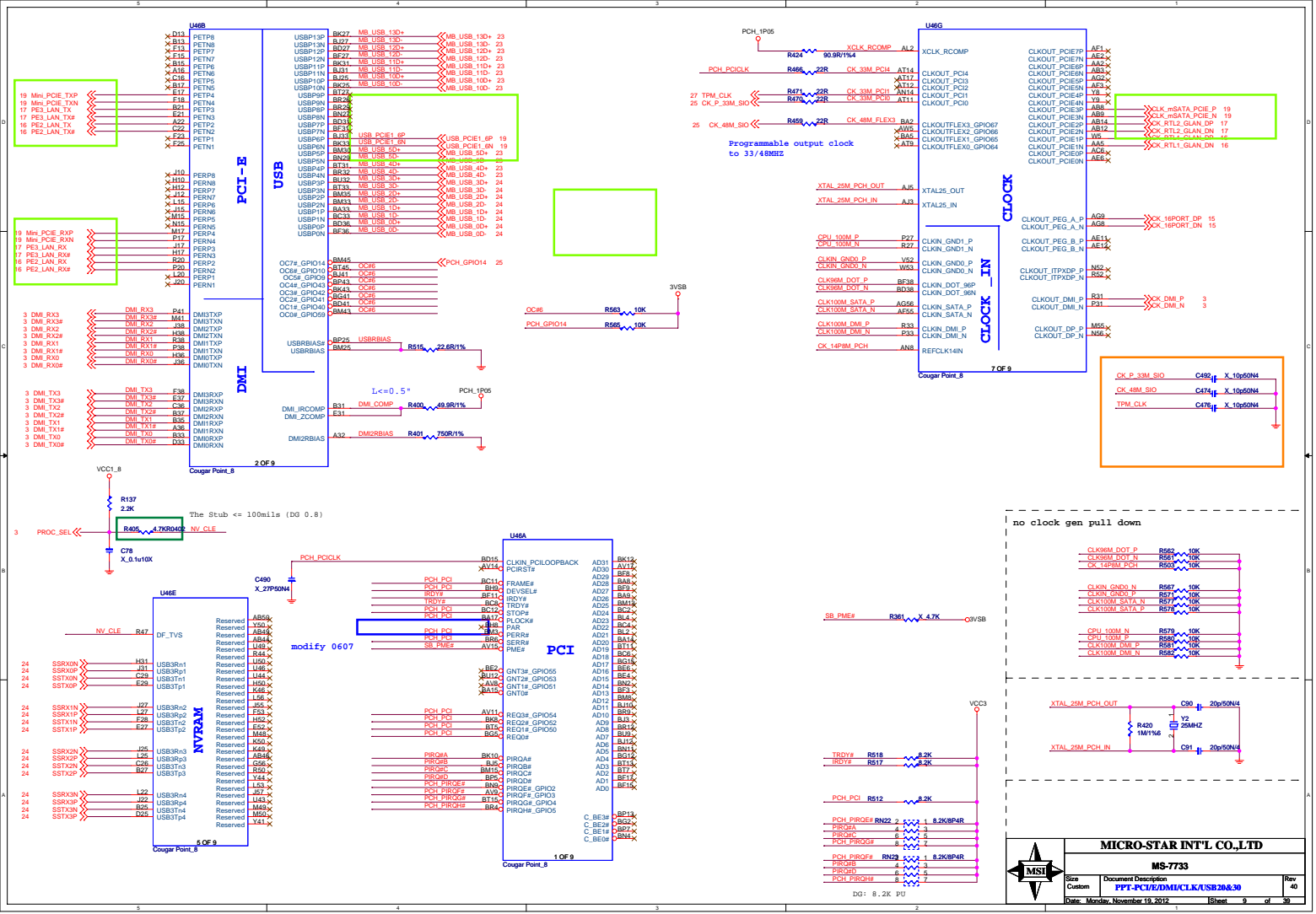
LGAT155

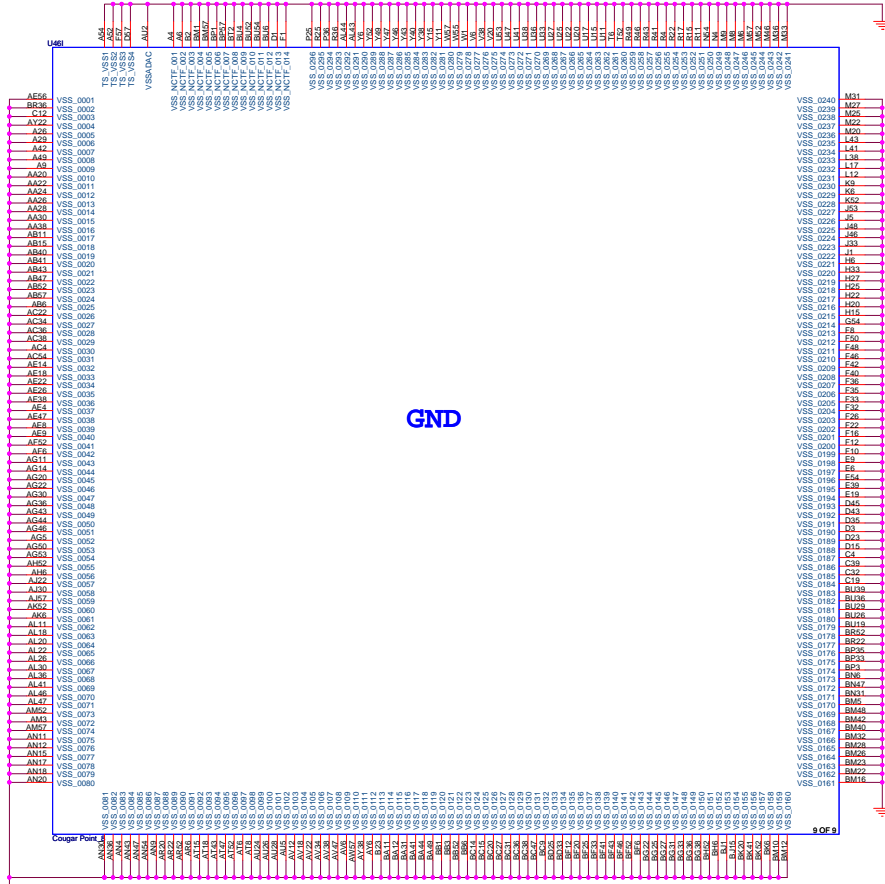
CPU#1
11 OF 11

X40	RSVD_001	RSVD_036	L33
X40	RSVD_002	RSVD_037	L33
X40	RSVD_003	RSVD_038	L33
X40	RSVD_004	RSVD_039	L33
X40	RSVD_005	RSVD_040	N33
X40	RSVD_006	RSVD_041	N33
X40	RSVD_007	RSVD_043	P33
X40	RSVD_008	RSVD_044	P33
X40	RSVD_009	RSVD_046	R33
X40	RSVD_010	RSVD_048	R33
X40	RSVD_011	RSVD_047	R33
X40	RSVD_012	RSVD_048	R40
X40	RSVD_013	RSVD_050	U33
X40	RSVD_014	RSVD_051	U33
X40	RSVD_015	RSVD_052	U33
X40	RSVD_016	RSVD_053	U33
X40	RSVD_017	RSVD_053	U33
X40	RSVD_018	RSVD_053	U33
X40	RSVD_019	RSVD_053	U33
X40	RSVD_020	RSVD_053	U33
X40	RSVD_021	RSVD_053	U33
X40	RSVD_022	RSVD_053	U33
X40	RSVD_023	RSVD_053	U33
X40	RSVD_024	RSVD_053	U33
X40	RSVD_025	RSVD_053	U33
X40	RSVD_026	RSVD_053	U33
X40	RSVD_027	RSVD_053	U33
X40	RSVD_028	RSVD_053	U33
X40	RSVD_029	RSVD_053	U33
X40	RSVD_030	RSVD_053	U33
X40	RSVD_031	RSVD_053	U33
X40	RSVD_032	RSVD_053	U33
X40	RSVD_033	RSVD_053	U33
X40	RSVD_034	RSVD_053	U33
X40	RSVD_035	RSVD_053	U33

LGAT155







PCH Straps



SPKR
0 : Default Mode:
1 : No Reboot Mode with TCO Disabled:



Internal pull-up
Do not pull low.



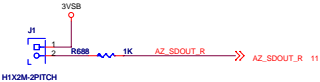
HDA_SYNC
OD PLL V# SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY
Internal weak pull down. Do not pull up.



Enable TLS:GPIO15
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.



BTM
Leave floating. Do not pull low.
FCIM
Pull low with 1k Ohm to ground.
FCIM. Can be override by
softstrap through ME.



Default
Do not pull high.
Disable ME in Manufacturing Mode
Connect to VccSusHDA with 1k Ohm pull-up
resistor through a jumper.

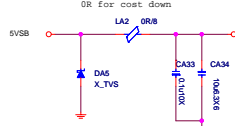
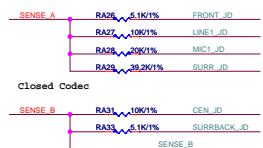
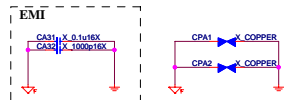
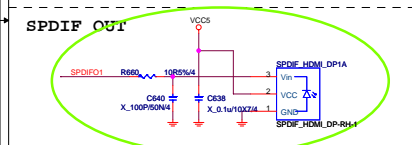
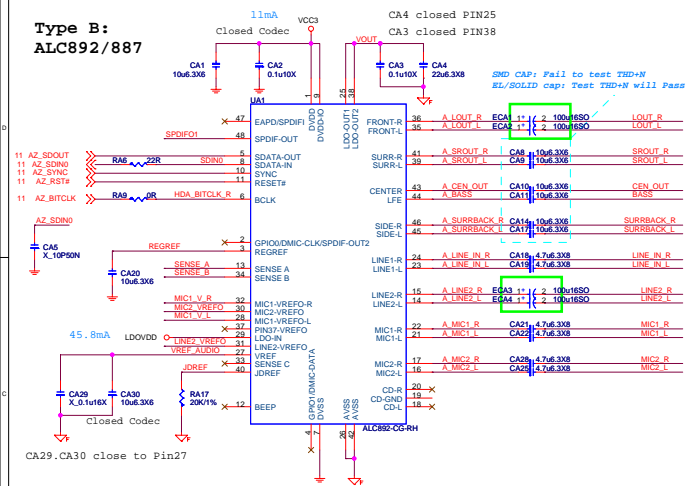


Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) - Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP - Use 8.2K-10K pull-down to ground.

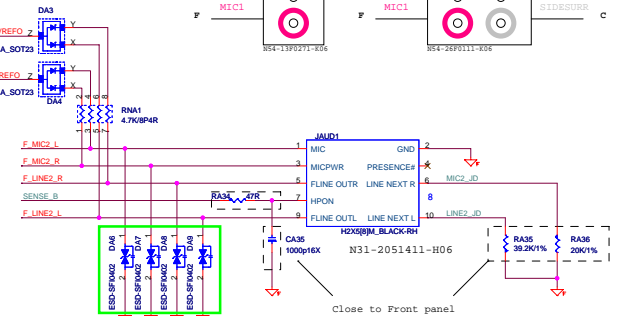
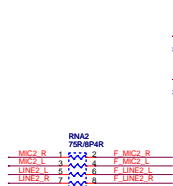
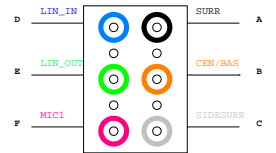
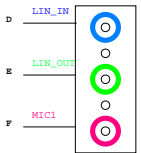
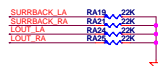
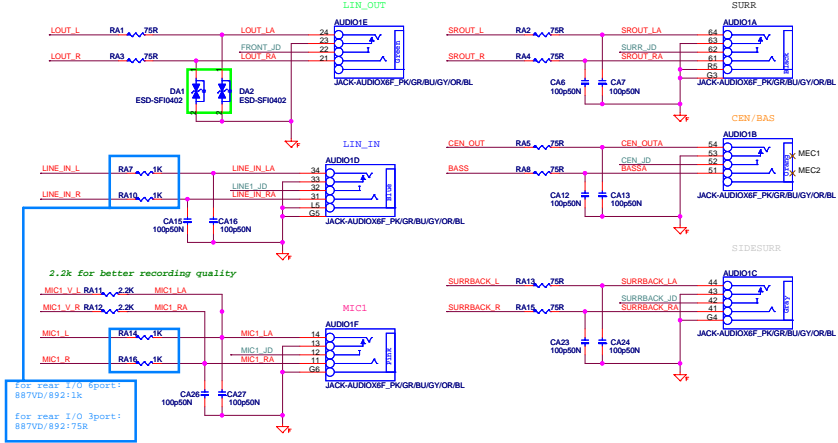


Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) - Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP - Use 8.2K-10K pull-down to ground.

Type B:
ALC892/887



CA33,CA34 close to LA1



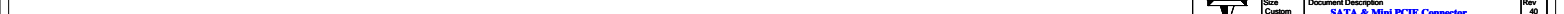
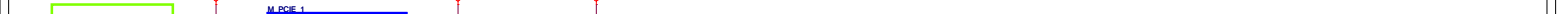
Varister --> cap for cost down
D0G-2950500-SI0
D0G-3010510-I05
Close to Jack



MICRO-STAR INT'L CO.,LTD

MS-7733

Size Custom	Document Description AUDIO 892	Re
Date: Tuesday, November 20, 2012		Sheet 18 of 39



Date: Tuesday, November 20, 2012 Sheet 19 of 39

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

10 DVI_DDPB_CLK_N
10 DVI_DDPB_CLK_P
10 DVI_DDPB_TXN0
10 DVI_DDPB_TXP0
10 DVI_DDPB_TXN1
10 DVI_DDPB_TXP1
10 DVI_DDPB_TXN2
10 DVI_DDPB_TXP2

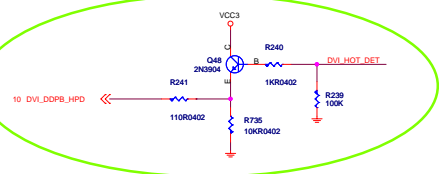
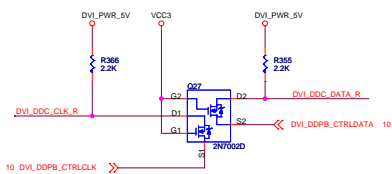
DVI_C_CLK_N
DVI_C_CLK_P
DVI_C_DATA0_N
DVI_C_DATA0_P
DVI_C_DATA1_N
DVI_C_DATA1_P
DVI_C_CLK_N
DVI_C_CLK_P
DVI_C_DATA2_N
DVI_C_DATA2_P

C337 0.1u10X
C336 0.1u10X
C362 0.1u10X
C361 0.1u10X
C338 0.1u10X
C339 0.1u10X
C364 0.1u10X
C363 0.1u10X

DVI_C_CLK_N
DVI_C_CLK_P
DVI_C_DATA0_N
DVI_C_DATA0_P
DVI_C_DATA1_N
DVI_C_DATA1_P
DVI_C_CLK_N
DVI_C_CLK_P
DVI_C_DATA2_N
DVI_C_DATA2_P

R499
R498
R497
R496
R495
R494
R493
R492

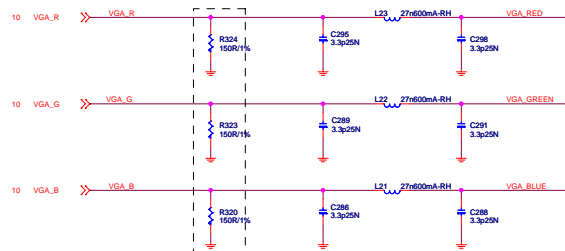
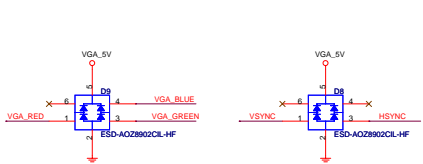
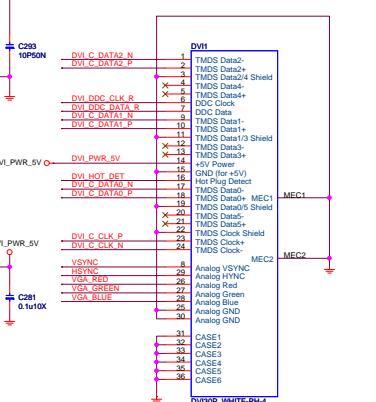
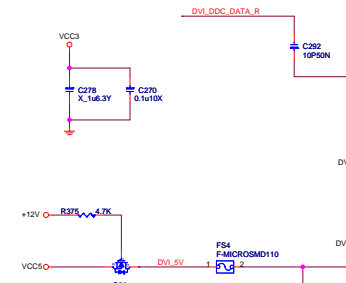
DVI_DATA_CLK_DP
DVI_DATA_CLK_DP
DVI_DATA0_N
DVI_DATA0_P
DVI_DATA1_N
DVI_DATA1_P
DVI_DATA2_N
DVI_DATA2_P



For EMI

DVI_C_DATA0_N
DVI_C_DATA0_P
DVI_C_DATA1_N
DVI_C_DATA1_P
DVI_C_CLK_N
DVI_C_CLK_P
DVI_C_DATA2_N
DVI_C_DATA2_P

R871 X_243R/1%
R874 X_243R/1%
R873 X_243R/1%
R872 X_243R/1%

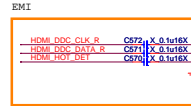
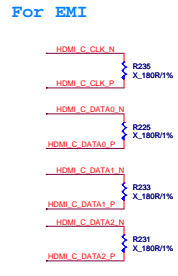
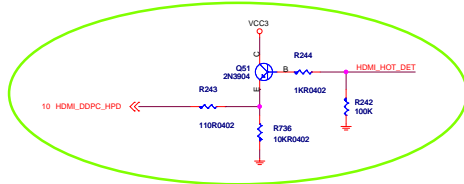
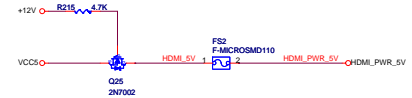
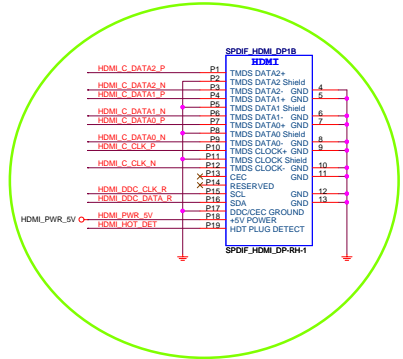
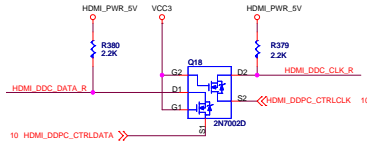
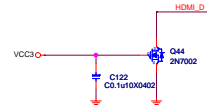


PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL. OF PIN



HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

10 HDMI_DDPCK_CLK_P	HDMI_DDPCK_CLK_P	C140	0.1u10X	HDMI_C_CLK_P	R545	80R	HDMI_D
10 HDMI_DDPCK_CLK_N	HDMI_DDPCK_CLK_N	C142	0.1u10X	HDMI_C_CLK_N	R546	80R	HDMI_D
10 HDMI_DDPCK_T2_P	HDMI_DDPCK_T2_P	C143	0.1u10X	HDMI_C_DATA2_P	R547	80R	HDMI_D
10 HDMI_DDPCK_T2_N	HDMI_DDPCK_T2_N	C144	0.1u10X	HDMI_C_DATA2_N	R548	80R	HDMI_D
10 HDMI_DDPCK_T1_P	HDMI_DDPCK_T1_P	C145	0.1u10X	HDMI_C_DATA1_P	R549	80R	HDMI_D
10 HDMI_DDPCK_T1_N	HDMI_DDPCK_T1_N	C146	0.1u10X	HDMI_C_DATA1_N	R550	80R	HDMI_D
10 HDMI_DDPCK_TX1_P	HDMI_DDPCK_TX1_P	C147	0.1u10X	HDMI_C_DATA0_P	R551	80R	HDMI_D
10 HDMI_DDPCK_TX1_N	HDMI_DDPCK_TX1_N	C148	0.1u10X	HDMI_C_DATA0_N	R552	80R	HDMI_D
10 HDMI_DDPCK_TX3_P	HDMI_DDPCK_TX3_P	C149	0.1u10X	HDMI_C_DATA0_P	R553	80R	HDMI_D
10 HDMI_DDPCK_TX3_N	HDMI_DDPCK_TX3_N	C151	0.1u10X	HDMI_C_DATA0_N	R554	80R	HDMI_D

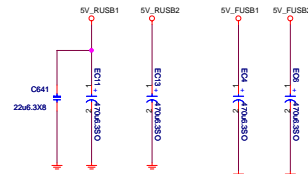
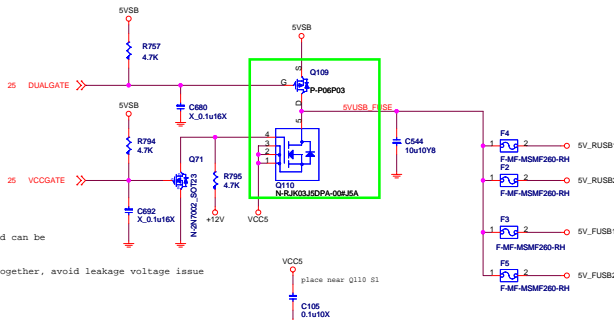


USB2.0/PS2 POWER Control				
MODE	S5	S0	S3	
S3P5_Gate#	1	1	1	
S0P5_Gate#	1	1	0	

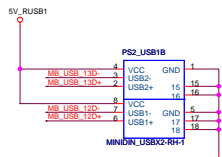
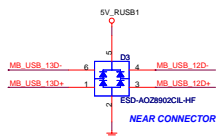
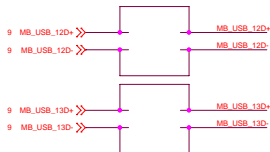
USB2.0/PS2 POWER Control				
MODE	S5	S0	S3	
S3P5_Gate#	0	1	1	
S0P5_Gate#	1	1	0	

*In S5# (S3P5_Gate# pin status is Tri-state, and can be programmed Low level.

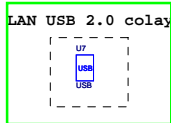
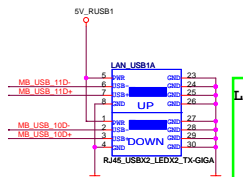
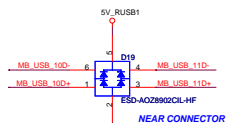
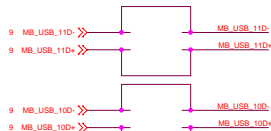
*S3P5_Gate# and S0P5_Gate# can't setting to low together, avoid leakage voltage issue



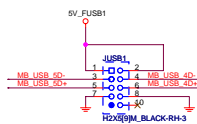
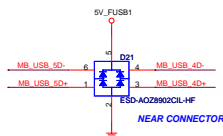
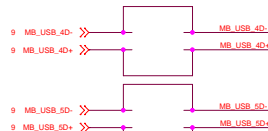
REAR USB PORT 12,13

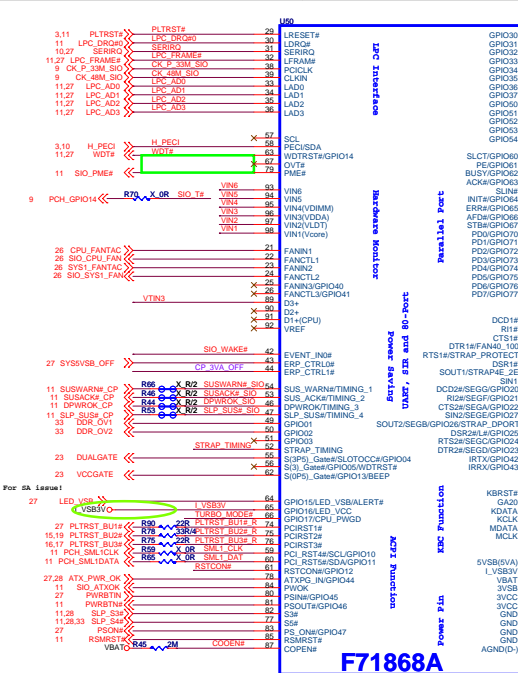


FRONT USB PORT 10,11(With LAN)



FRONT USB PORT 4.5

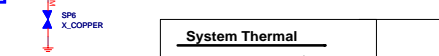
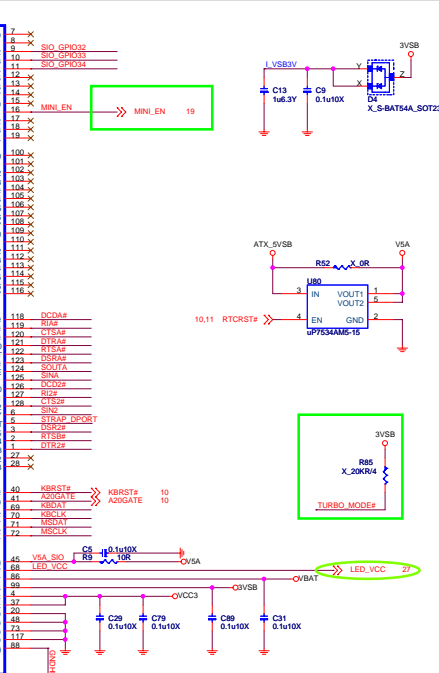
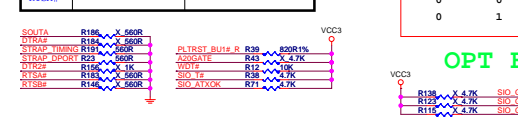




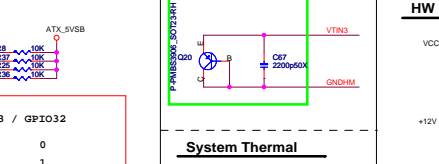
USB_MODE
Hi by BIOS programming,
default h/w PD for avoid U7536 Enable pin floating

LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

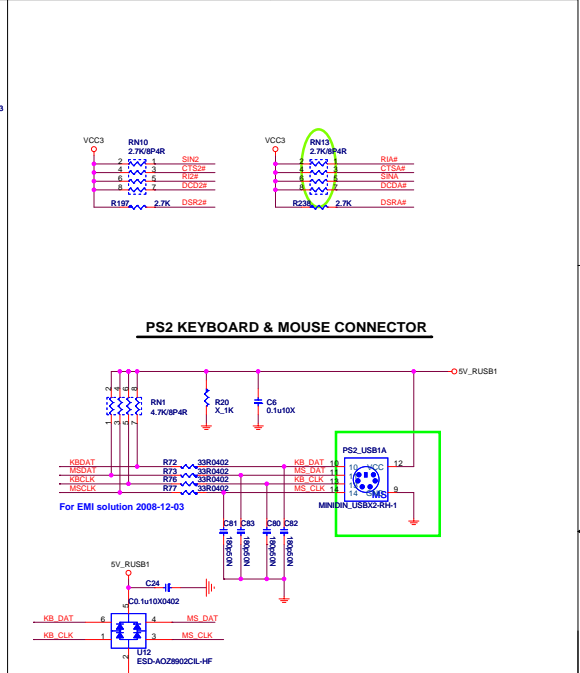
STRAP	Don't STUFF	STUFF
SOUTA#	4E	2E
WTR#A	FAN START DUTY 40%	FAN START DUTY 100%
STRAP	AMD Timing	Intel Cougar point Timing
TIMING		
FANCTL1 1/2/3	DAC Mode	IPWM Mode
STRAP	Enable 80 Port	Disable 80 Port
WTR#B (SOUT2)		
RTSA#		



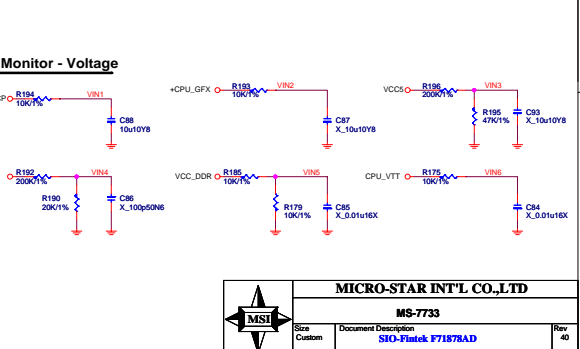
System Thermal



System Thermal



HW Monitor - Voltage



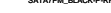
3.0 Black



3.0 Black



2.0 Black



FAN-COUNTROL CIRCUIT



SYSTEM FAN1



MS-7733

Size Custom	Document Description FAN Control	Rev 40
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VRMPGRD LEVEL SHIFT

CPU_VTT, 3VSB, VCC3, VRM_PGD_R, R29, R4, R5, C10, Q1, NPN CURT3904.

UPI VOLTAGE CONSOLE

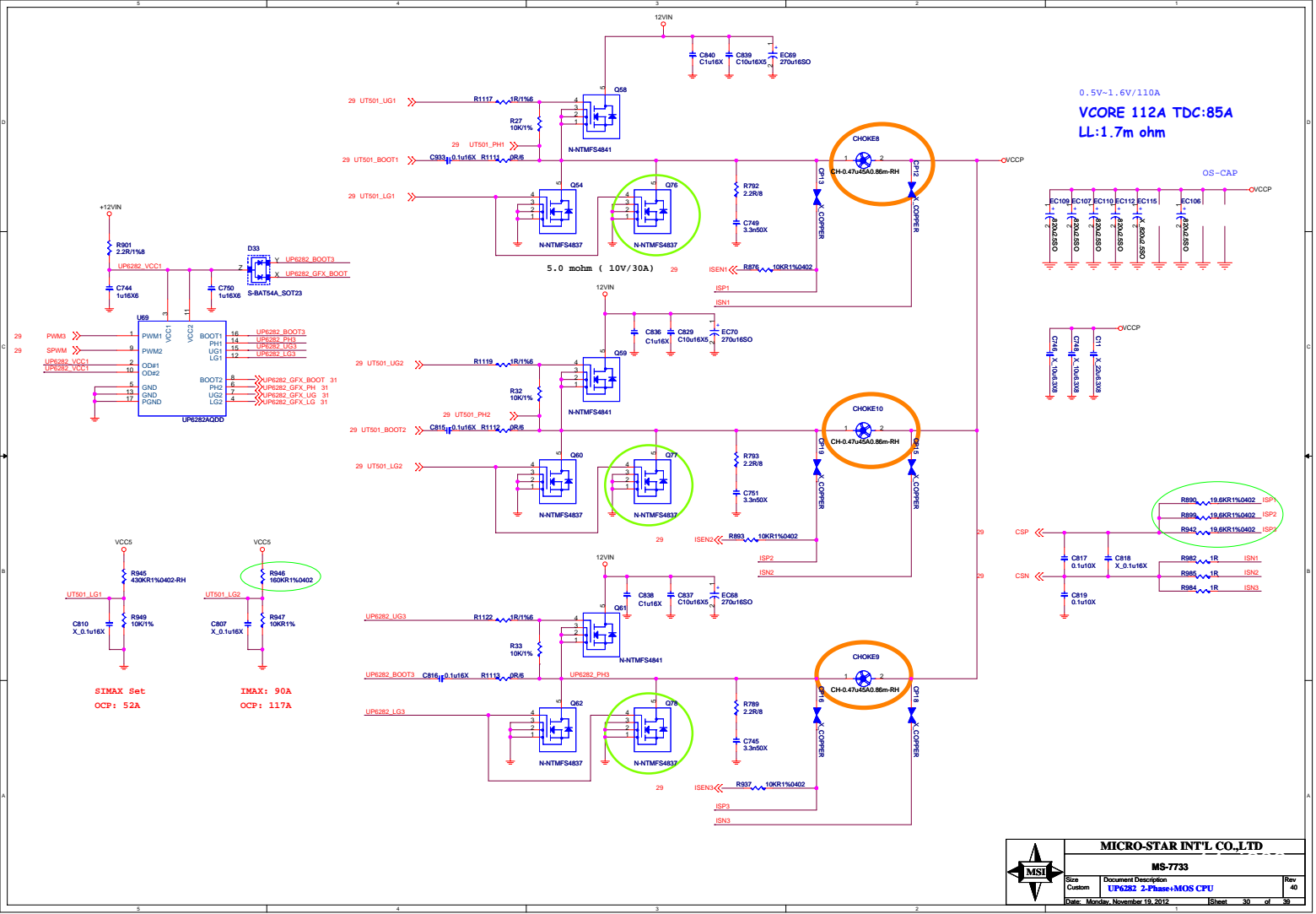
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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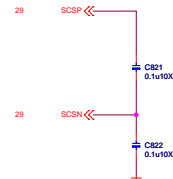
MS-7733

Rev: Custom Document Description: VRM112 - UT501 Date: Marlow, November 19, 2012 IS Item: 29 of 39

<u>UPI VOLTAGE CONSOLE</u>						
0x20:RH=10K,RL=OPEN						
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	0	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



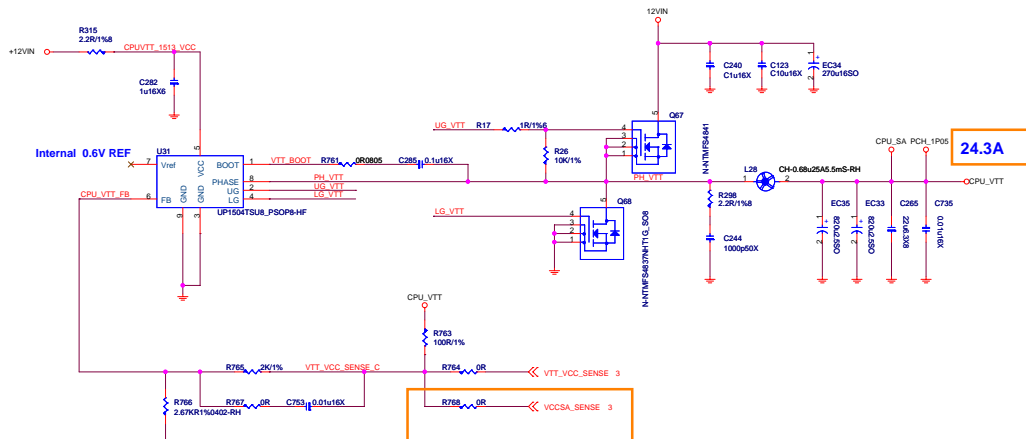
35A FOR CPU



$$5 \times 1 = 5A > 3.8A$$

Iripple=6.2
4.7*1A<6.2A share with VCCP

Acture measure cpu_vtt max 10A
Iripple=2.55A



VTT SELECT Remove

DDR Power:1.5V

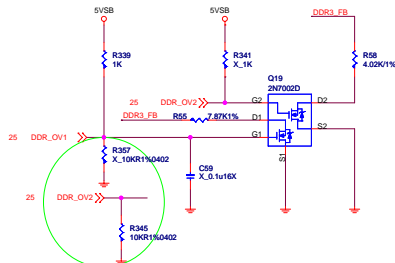
DDR3_1.5V 4.75A+5.5A+0.5A=10.75A

4.75A FOR CPU

5.5A FOR 4DIMM

0.5A FOR DDR VTT

DDR OV

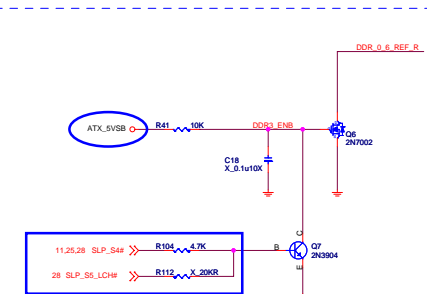


*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

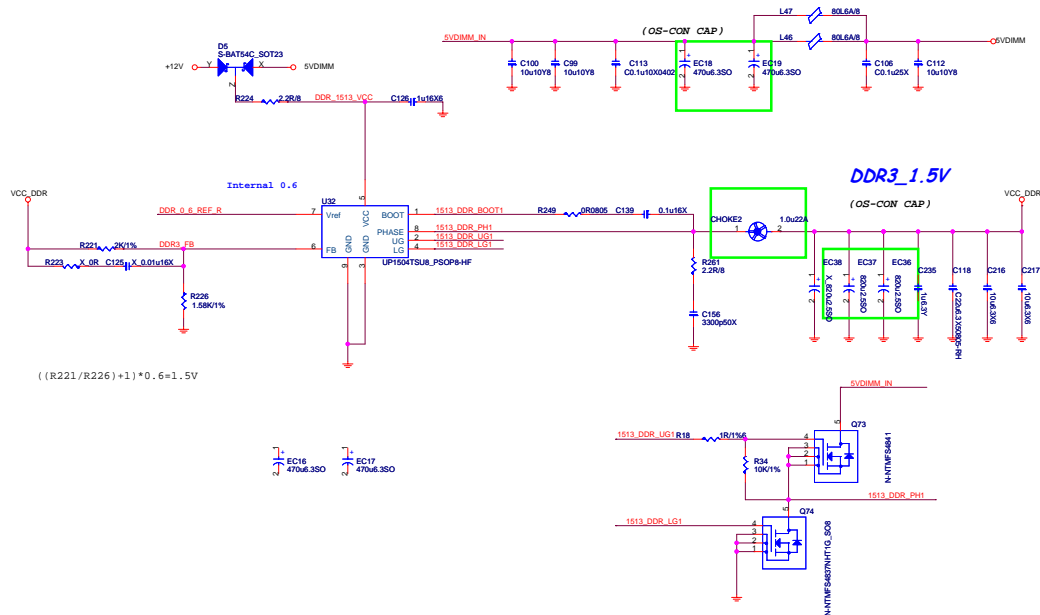
DDR_OV1 = GPIO01(S/I/O)

DDR_OV2 = GPIO02(S/I/O)



P.S. Only for meet Intel power down sequence.

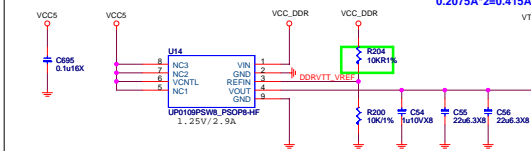
Iripple=4.868
3*2*1=6A>4.868A



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.2075A*2=0.415A



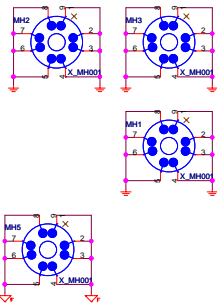
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MS-7733

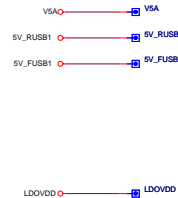
Rev	Document Description	Rev
40	UPLSMT - DDR POWER	40

Date: Tuesday, November 20, 2012 15:00:33 of 39

Mounting Holes



Voltage test point

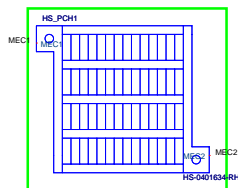
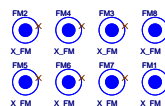


VCCP	VCCP
+CPU_GFX	+CPU_GFX
CPU_SA	CPU_SA
VCC_DDR	VCC_DDR
VTT_DDR	VTT_DDR
PCH_1P05	PCH_1P05
VCC1_8	VCC1_8
SVDIMM	SVDIMM
+12V	+12V
VCC5	VCC5
VCC3	VCC3
ATX_5VSB	ATX_5VSB
5VSB	5VSB
3VSB	3VSB
VBAT	VBAT
3VA	3VA

Simulation



Optical Fiducial Marks-120



5

4

3

2

1

EMI:cap. for signal return path

EMI

EMI

D

D

C


C

B

B

A

A

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	MS-7733		
	Size	Document Description	Rev
	Custom	EMI CAP	40
Date: Monday, November 12, 2012		Sheet	35 of 35